What is Claimed is:

1. A method comprising:

routing a first pair of input signals and a second pair of input signals to circuitry that is concentrated in a particular area of a programmable logic resource;

applying a multiply operation to the second pair of input signals using the circuitry;

applying a feedback output to the circuitry, wherein the feedback output is set to zero;

concatenating each signal of the first pair of input signals and the feedback output; and

applying an accumulate operation on a result of the multiply operation with a result of the concatenating.

2. The method of claim 1 further comprising setting the first pair of input signals to zero.

3. The method of claim 2 wherein applying the accumulate operation comprises one of:

adding the result of the multiply operation to the result of the concatenating; and

subtracting the result of the multiply operation from the result of the concatenating.

4. The method of claim 1 further comprising:

setting the first pair of input signals to values that when concatenated in a predetermined order, comprises a first predetermined number of most significant bits of an initialization value; and

setting the second pair of input signals to values such that the result of the multiply

operation comprises a second predetermined number of least significant bits of the initialization value.

5. The method of claim 4 wherein the first predetermined number and the second predetermined number comprise the initialization value.

6. The method of claim 4 wherein the feedback output has a number of bits equal to the second predetermined number.

7. The method of claim 4 wherein applying the accumulate operation comprises adding the result of the multiply operation to the result of the concatenating.

8. A method comprising:

routing a pair of input signals to circuitry that is concentrated in a particular area of a programmable logic resource;

applying a multiply operation to the pair of input signals using the circuitry;

clearing a register in the circuitry based on at least one dedicated configuration bit that is set;

applying a feedback output to the circuitry, wherein the feedback output is set to zero;

concatenating contents of the register with the feedback output; and

applying an accumulate operation on a result of the multiply operation with a result of the concatenating.

9. The method of claim 8 wherein the dedicated configuration bit is set by user input.

10. The method of claim 8 wherein applying the accumulate operation comprises one of:

adding the result of the multiply operation to the result of the concatenating; and

subtracting the result of the multiply operation from the result of the concatenating.

11. A multiplier-accumulator block operative to zero or initialize an accumulator value with minimal clock latency comprising:

a first multiplier having a first input operative to receive a first input signal, a second input operative to receive a second input signal, and an output;

a second multiplier having a first input operative to receive a third input signal, a second input operative to receive a fourth input signal, and an output;

an accumulator having a first input operative to receive the output of the first multiplier, a second input operative to receive the output of the second multiplier, a third input operative to receive a feedback output, and an output, wherein the feedback output is set to zero; and

a register block having an input operative to receive the output of the accumulator and an output.

12. The multiplier-accumulator block of claim 11 wherein the second multiplier applies a multiply operation on the third input signal and the fourth input signal, wherein a result of the multiply operation is sent to the output.

13. The multiplier-accumulator block of claim 11 wherein the first input signal and the second input signal are concatenated in a predetermined order and sent directly to the output of the first multiplier.

14. The multiplier-accumulator block of claim 11 wherein the first input signal and the second input signal are both set to zero.

15. The multiplier-accumulator block of claim 14 wherein the accumulator:

concatenates the feedback output to the output of the first multiplier to generate the accumulator value; and

adds the output of the second multiplier to the accumulator value.

16. The multiplier-accumulator block of claim 14 wherein the accumulator:

concatenates the feedback output to the output of the first multiplier to generate the accumulator value; and

subtracts the output of the second multiplier from the accumulator value.

17. The multiplier-accumulator block of claim 11 wherein:

the first input signal and the second signal are set to values such that the output of the first multiplier comprises a first predetermined number of most significant bits of the accumulator value; and

the third input signal and the fourth input signal are set to values such that the output of

the second multiplier comprises a second predetermined number of least significant bits of the accumulator.

18. The multiplier-accumulator block of claim 17 wherein the feedback output has a number of bits equal to the second predetermined number.

19. The multiplier-accumulator block of claim 17 wherein the accumulator:

concatenates the feedback output to the output of the first multiplier to generate a concatenated value; and

adds the output of the second multiplier to the concatenated value to generate the accumulator value.

20. A programmable logic resource comprising the multiplier-accumulator block of claim 11.

21. A digital processing system comprising:

processing circuitry;

a memory coupled to the processing circuitry; and

a programmable logic resource as defined in claim 20 coupled to the processing circuitry and the memory.

22. A printed circuit board on which is mounted a programmable logic resource as defined in claim 20.

23. The printed circuit board defined in claim 22 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic resource.

24. The printed circuit board defined in claim 23 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable logic resource.